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Journal of the European Ceramic Society 27 (2007) 3935–3939
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Complex impedance spectroscopy study of a liquid-phase-sintered α-SiC ceramic

José Sánchez-González [a,*], Angel L. Ortiz [a], Fernando Guiberteau [a], Carmen Pascual [b]

[a] Departamento de Electrónica e Ingeniería Electromecánica, Escuela de Ingenierías Industriales, Universidad de Extremadura, 06071 Badajoz, Spain
[b] Departamento de Electrocerámica, Instituto de Cerámica y Vidrio, Consejo Superior de Investigaciones Científicas, Kelsen 5, 28049 Madrid, Spain

Available online 5 April 2007

Abstract

The electrical response of a liquid-phase-sintered (LPS) α-SiC with 10 wt.% $Y_3Al_5O_{12}$ (YAG) additives was studied from near-ambient temperature up to 800 °C by complex impedance spectroscopy. The electrical conductivity of this LPS SiC ceramic was found to increase with increasing temperature, which was attributed to the semiconductor nature of the SiC grains. It was concluded that the contribution of the SiC grains to the electrical conductivity of the LPS SiC ceramic at moderate temperatures (<450 °C) is a somewhat greater than that of the YAG phase. In contrast, at higher temperatures the SiC grains control the electrical conductivity of the LPS SiC ceramic. It was also found that there are two activation energies for the electrical conduction process of the α-SiC grains. These are 0.19 eV at temperatures lower than ∼400 °C and 2.96 eV at temperatures higher than ∼500 °C. The existence of two temperature-dependence conduction regimes reflects the core–shell substructure that develops within the SiC grains during the liquid-phase sintering, where the core is pure SiC (intrinsic semiconductor) and the shell is mainly Al-doped SiC (extrinsic semiconductor).

Keyword: Impedance spectroscopy; SiC; Liquid-phase sintering; Electrical properties

1. Introduction

Silicon carbide (SiC) is a semiconductor material with physic-chemical properties of great interest for the electronics industry. In particular, SiC has a wide bandgap (∼2.4–3.3 eV, depending on the polytype),[1] and high values of the breakdown electric field ($\sim 2–4 \times 10^6$ V cm^{-1}),[1] saturation drift velocity ($\sim 2 \times 10^7$ cm s^{-1}),[1] thermal conductivity (∼5 kW cm^{-1} °C),[2] and melting point (>3000 °C).[3] Furthermore, SiC is inherently hard, stiff, lightweight, chemically inert and resistant to creep and wear, all desirable properties in functional applications. It is not surprising therefore that it has been suggested that SiC could revolutionize electronics technology, because the semiconductor devices made of SiC would operate safely in hostile environments and at high temperatures that other semiconductors cannot tolerate.

Usually, high-quality wafers are used to fabricate semiconductor devices. Although steady progress has been made over recent years in the growth of SiC single-crystals, there are still several critical issues related with the elimination of crystal and surface defects that need to be resolved prior to the mass production of high-quality SiC wafers. Parallel to the efforts in improving the growth methods of SiC single-crystals, there is also a strong motivation to investigate the electrical response of SiC polycrystals, as this would provide cheaper forms of SiC for the fabrication of semiconductor devices. In this context, there is only limited interest in solid-state-sintered SiC polycrystals, again due to the serious processing difficulties and high production costs. Typically, pressureless liquid-phase sintering has been used for low-cost processing of SiC ceramics.[4–6] While there is extensive knowledge on the mechanical properties of the liquid-phase-sintered (LPS) SiC ceramics, little is known about their electrical properties and how they correlate with the microstructure.[7–11]

Thus, the objective of the present work was to study the electrical response of a typical LPS SiC from near-ambient temperature up to 800 °C by complex impedance spectroscopy, and to connect the electrical properties to the microstructure. Here we show that LPS SiC ceramics have promise as electroceramics, and suggest that their interesting electrical properties could be tailored by microstructural control.

* Corresponding author.
E-mail address: jsg@unex.es (J. Sánchez-González).

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doi:10.1016/j.jeurceramsoc.2007.02.066

2. Experimental procedure

2.1. Processing

α-SiC powder (UF-15, H.C. Starck., Goslar, Germany) with 4.29 wt.% Al_2O_3 (AKP-30, Sumitomo Chemical Company, New York, NY, USA) and 5.71 wt.% Y_2O_3 (Fine Grade, H.C. Starck, Goslar, Germany) as additives was ball-milled for 24 h in ethanol using ZrO_2 balls. This batch composition yields an LPS SiC ceramic with 7.3 vol% $Y_3Al_5O_{12}$ (YAG) after sintering. The slurry was dried, and the resulting powder de-agglomerated and sieved. A compact was made by uniaxial pressing (C, Carver Inc., Wabash, IN, USA) at 50 MPa, followed by isostatic pressing (CP360, AIP, Columbus, OH, USA) at 350 MPa. Sintering was performed (1000-3560-FP20, Thermal Technology Inc., Santa Rosa, CA, USA) at 1950 °C for 1 h in a flowing Ar-gas atmosphere, without external pressure. Additional details of the processing procedure have been given elsewhere.[4–6]

2.2. Microstructural characterization

The density of the sintered ceramic was measured using Archimedes' method, with distilled water as the immersion medium. Cross-sections of the LPS SiC ceramic were polished to a 1 μm finish and plasma-etched (PT 1750, Fissions Instruments, East Sussex, UK) with CF_4 gas, and were then observed under the SEM (S-3600N, Hitachi, Japan). Grain morphology analysis was performed from different SEM micrographs by image analysis on no less than 300 grains.

2.3. Electrical characterization

A plate specimen (8 mm in square and 2 mm in thickness) was machined out of the sintered disc, and all specimen faces were polished to a 1 μm finish. The impedance data of the LPS SiC ceramic as a function of the temperature were collected from the same sample in an increasing temperature sequence. The measurements were performed using a Solartron 1255 HF frequency response analyzer equipped with a Solartron 1286 electrochemical interface. The measurement conditions were: frequency range 0.1 Hz–1 MHz, temperature range 40–800 °C, AC amplitude 50 mV, two electrodes painted with Pt paste, and flowing Ar-gas atmosphere. The analysis of the impedance data was carried out using the Zview software (Scribner Associates Inc., USA), which allows the values of the equivalent circuit components to be determined.

3. Results and discussion

Shown in Fig. 1 is a representative SEM micrograph of the LPS SiC ceramic studied here. The absence of residual porosity in the SEM image indicates that the ceramic is fully dense, which is consistent with the 3.310 ± 0.001 g cm^{-3} density value measured directly by Archimedes' method. With respect to the microstructure of the LPS SiC ceramic, it can be observed in Fig. 1 that the grains have almost equiaxed form (the mode aspect ratio is 1.3 ± 0.1) and size within the ultrafine scale (the mode grain size is 0.6 ± 0.1 μm). The intergranular phase is fully crystalline YAG, as determined using X-ray diffraction analysis,[12,13] and is mostly distributed at pockets located at triple points of the grain structure. An amorphous film with thickness of various nanometers is also present at the grain boundaries.

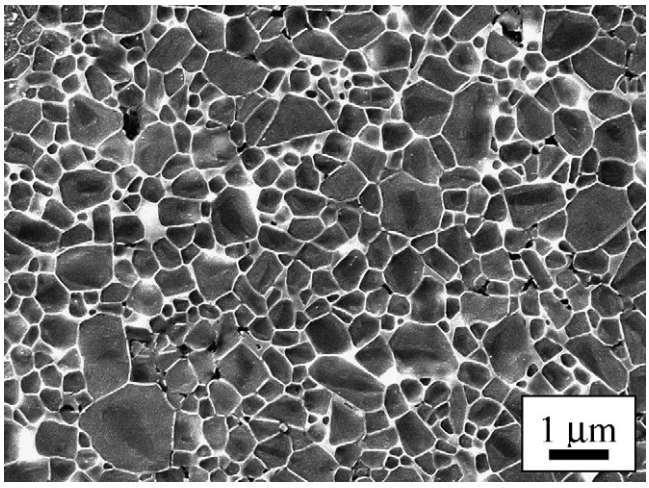

Fig. 1. SEM micrograph of a polished and plasma-etched cross-section of the LPS SiC ceramic. The dark and light regions are the SiC grains and the YAG phase, respectively.

Cole–Cole curves obtained from 40 °C up to 800 °C for the LPS SiC ceramic are shown in Fig. 2A–D. It can be observed that, regardless of the temperature, there are two contributions to the electrical response of the LPS SiC ceramic, a fact that differential impedance analysis (not shown) confirmed. Up to ∼250 °C, the two contributions overlap severely, resulting in a single deformed arc in the Cole–Cole curve. At ∼250 °C, the two contributions begin to split, giving two partially overlapped arcs in the Cole–Cole curve. With increasing temperature, the degree of overlap between the two contributions decreases, and above ∼450 °C they are entirely resolved giving two discernible arcs in the Cole–Cole curve. The existence of two contributions to the electrical response of the LPS SiC ceramic reflects the two-phase nature of this material, which consists of SiC grains and YAG intergranular phase (see Fig. 1). In this context, the low-frequency arc is attributed to the YAG phase and grain boundaries,[14] whereas the high-frequency arc is attributed to the SiC grains.[14]

Another observation that can be made from Fig. 2 is that the real part of the impedance decreases continuously with increasing temperature, which is much more pronounced for the high-frequency arc. This trend indicates that the electrical conductivity of the SiC grains increases with increasing temperature, as one would expect since SiC is a semiconductor material.

The brick layer model provides the typical framework to analyze the impedance data of polycrystalline ceramics,[15] and therefore will be the one used here. The utility of this model is that it allows the electrical conductivity of the different phases in the sample to be calculated on the basis of a circuit model whose theoretical electrical response matches the experimental impedance spectroscopy data. Given that there are two phases

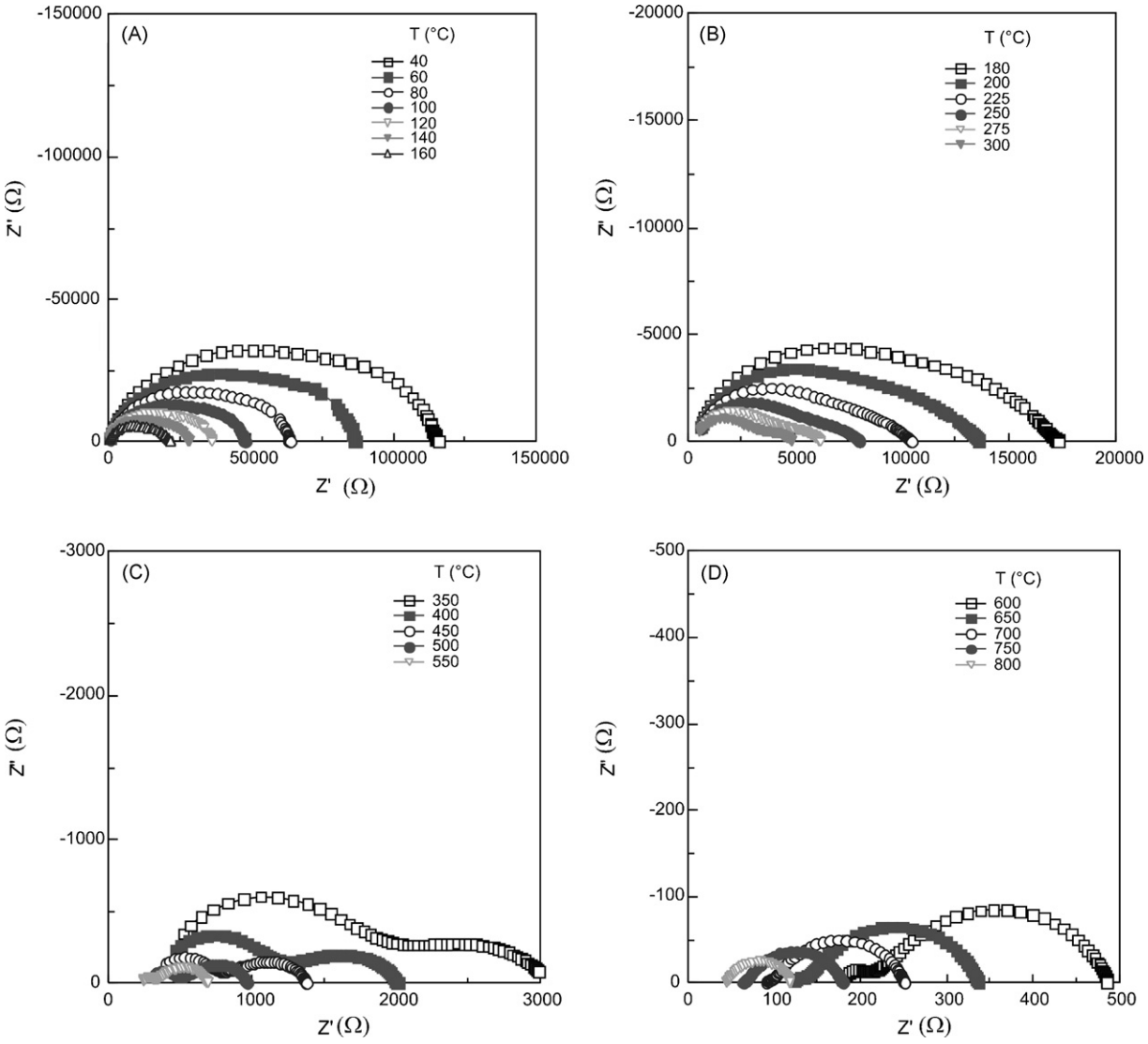

Fig. 2. Cole–Cole plots of the LPS SiC ceramic in the temperature range: (A) 40–160 °C, (B) 180–300 °C, (C) 350–550 °C and (D) 600–800 °C. The figure has been separated in four for the sake of clarity.

contributing to the experimentally observed electrical response of the LPS SiC ceramic, we selected the two parallel R-CPE (constant phase element) in-series circuit shown in Fig. 3. For each temperature, the values of the circuit components are obtained by a non linear least-squares fitting procedure. Once the values for the resistances (R) are determined, the electrical conductivities (σ) can be calculated by the expression $\sigma = h/(RA)$,

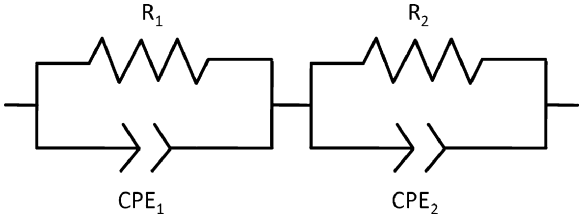

Fig. 3. Two parallel R-CPE (constant phase element) in-series circuit used to model the experimental impedance data.

where h and A are the thickness and area of the LPS SiC plate, respectively. Shown in Fig. 4 is the Neperian logarithm of electrical conductivity of the two phases as a function of the inverse of the temperature (the Arrhenius plot). The following interesting features stand out in this figure: (1) the electrical conductivity of the SiC and YAG phases increases with increasing temperature, (2) the electrical conductivity of the SiC grains is higher and more temperature-dependent than that of the YAG phase, (3) at moderate temperatures (<∼400 °C) the electrical conductivity of the LPS SiC ceramic is slightly more dependent on the SiC grains than on the YAG phase, whereas at high-temperatures (>∼500 °C) it is controlled by the SiC grains. These three observations can be understood by recalling that SiC is a wide-bandgap semiconductor whereas YAG is an electrical insulator.

With respect to the electrical conductivy of the SiC grains, it can be seen in Fig. 4 that there are two successive electrical conduction regimes: a first linear regime up to ∼400 °C where the

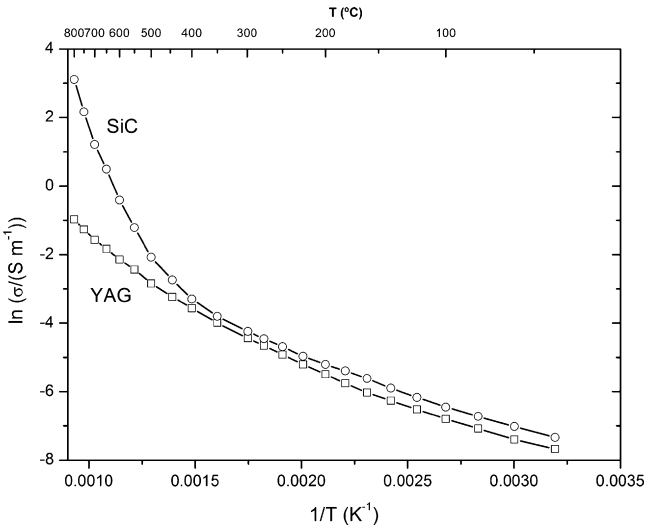

Fig. 4. Arrhenius plot of the conductivity of the LPS SiC ceramic in the temperature range 40–800 °C.

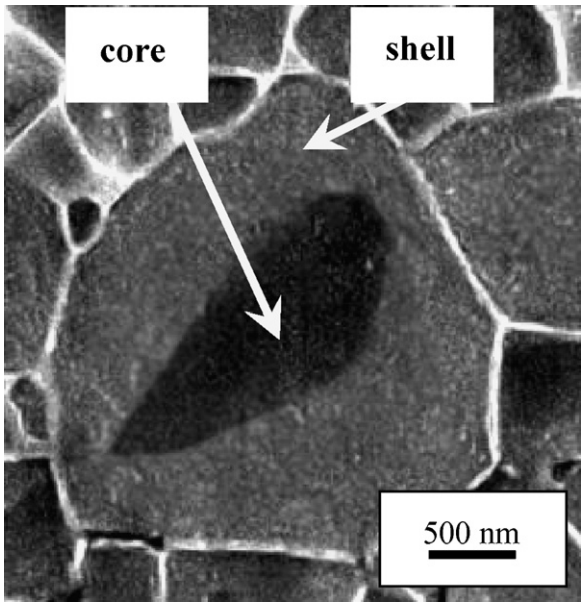

Fig. 5. SEM micrograph showing the internal details of the SiC grains in the LPS SiC ceramic. The core–shell substructure within the SiC grains is visible in the micrograph due to differential plasma etching. The dark and light regions are the core and the shell, respectively.

conductivity increases gradually with increasing temperature, which is followed by a smooth transition (at ~400–500 °C) to a second linear regime where the conductivity increases abruptly with increasing temperature. This type of behavior (two different linear regions) reflects the existence of two activation energies for the electrical conduction process of the SiC grains, which is a typical phenomenon of doped semiconductors (extrinsic and intrinsic responses). In particular, from the slopes of the two linear stretches we calculated that the activation energies for the electrical conduction process in the intrinsic (temperature >500 °C) and extrinsic (temperature <400 °C) zones are 2.96 and 0.19 eV, respectively. It is noted that the activation energy in the intrinsic zone is very close to the energy bandgap of the 6H polytype of SiC, which is ~3 eV.[16] This similarity is consistent with the composition of the starting SiC powder used to fabricate the LPS SiC ceramic,[4] which was measured to be 87% 6H and 13% 15R by Rietveld analysis of the X-ray diffraction pattern. Additionally, the activation energy in the extrinsic zone would be entirely consistent with the existence of substitutional Al in the SiC lattice, since Al is known to introduce an acceptor level with 0.2 eV energy within the bandgap of the 6H-SiC.[16]

To confirm that the cause of the existence of an extrinsic zone is the formation of substitutional solid-solutions with Al atoms as principal solutes in the SiC host, we performed detailed microstructural observations by SEM on the LPS SiC ceramic previously plasma-etched with CF_4 gas. The utility of this plasma-etching is that it is capable of revealing differences in the chemical composition within SiC grains. A representative high-magnification SEM image is shown in Fig. 5. A contrast within the SiC grains is visible, which is indicative of a core–shell substructure where the chemical compositions of the inner and outer parts are different. Since the average particle size of the SiC powder was 0.5 μm and the average grain size in the LPS SiC ceramic is 0.6 μm, the core and shell constitute about 80 and 20% of each grain, respectively. In particular, earlier studies have shown by energy-dispersive X-ray spectroscopy (EDXS) that the core is pure SiC[16] (and therefore an intrinsic semiconductor), whereas the shell is SiC with traces of Al, Y, and O[17] (and therefore an extrinsic semiconductor) incorporated from the liquid-stage intergranular phase during grain growth by solution-reprecipitation (Ostwald ripening). Most importantly, detailed analysis by EDXS coupled with high-resolution electron microscopy performed by others[18] has demonstrated that the principal solutes in the SiC host are indeed the Al atoms. The Al doping is thus deemed responsible for the existence of the extrinsic electrical conduction zone of the SiC grains in the LPS SiC ceramic.

In sum, we have shown that LPS SiC possesses interesting electrical properties, which, combined with the ease and economy of the pressureless processing, make it an attractive low-cost electroceramic material. In addition, the results suggest that the electrical response of LPS SiC could to be tailored by judicious selection of the percentage of sintering additives, the nature of those additives, the sintering atmosphere and time, and the type of SiC starting powder. This possibility will be explored in future studies.

4. Conclusions

We studied the electrical response of an LPS SiC ceramic processed with 10 wt.% Al_2O_3–Y_2O_3 additives from near-ambient temperature up to 800 °C by complex impedance spectroscopy. Based on this study, the following conclusions can be drawn:

- There are two contributions to the electrical conductivity of the LPS SiC ceramic, one from the SiC grains and the other from the YAG intergranular phase. The overall electrical conductivity increases with increasing temperature.
- With increasing temperature, the electrical conductivity of the SiC grains is increasingly greater than that of the YAG

intergranular phase, in accordance with the semiconductor nature of SiC grains and insulator nature of the YAG phase.
- There exist two activation energies for the electrical conduction process of the SiC grains (2.96 and 0.19 eV), a reflection of the core–shell substructure that the SiC grains develop during liquid-phase sintering. The core behaves as an intrinsic semiconductor and the shell as an extrinsic semiconductor.
- The interesting electrical properties of LPS SiC ceramics may be tailorable by microstructural control during sintering. If this is found to be so, then LPS SiC could be a promising low-cost electroceramic.

Acknowledgements

This work was supported by the Ministerio de Ciencia y Tecnología (Government of Spain) and the Fondo Europeo de Desarrollo Regional (FEDER) under grant nos. CICYT MAT 2004-05971 and UNEX00-23-013 and UNEX05-23-010.

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